EXHIBIT 22

[redacted]

UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

TQ DELTA, LLC, *Plaintiff,* v. **COMMSCOPE HOLDING COMPANY, INC., COMMSCOPE INC., ARRIS US HOLDINGS, INC., ARRIS SOLUTIONS, INC., ARRIS TECHNOLOGY, INC., and ARRIS ENTERPRISES, LLC** *Defendants.*	CIV. A. NO. 2:21-CV-310-JRG (Lead Case)
TQ DELTA, LLC, *Plaintiff,* v. **NOKIA CORP., NOKIA SOLUTIONS AND NETWORKS OY, and NOKIA OF AMERICA CORP.,** *Defendants.*	CIV. A. NO. 2:21-CV-309-JRG (Member Case)

OPENING EXPERT REPORT OF DR. RICHARD WESEL ON THE INVALIDITY OF THE ASSERTED CLAIMS OF THE FAMILY 3 PATENTS (U.S. PATENT NOS. 7,844,882; 8,276,048; 8,495,473; 9,547,608)

Table 8-2/G.993.1 – Example of interleaver parameters with RS(144,128)

Rate [kbit/s]	Interleaver parameters	Interleaver depth	(De)interleaver memory size	Erasure correction	End-to-end delay
50 × 1024	$I = 72$ $M = 13$	937 blocks of 72 bytes	33 228 bytes	3 748 bytes 520 µs	9.23 ms
24 × 1024	$I = 36$ $M = 24$	865 blocks of 36 bytes	15 120 bytes	1 730 bytes 500 µs	8.75 ms
12 × 1024	$I = 36$ $M = 12$	433 blocks of 36 bytes	7 560 bytes	866 bytes 501 µs	8.75 ms
6 × 1024	$I = 18$ $M = 24$	433 blocks of 18 bytes	3 672 bytes	433 bytes 501 µs	8.5 ms
4 × 1024	$I = 18$ $M = 16$	289 blocks of 18 bytes	2 448 bytes	289 bytes 501 µs	8.5 ms
2 × 1024	$I = 18$ $M = 8$	145 blocks of 18 bytes	1 224 bytes	145 bytes 503 µs	8.5 ms

The following interleaver parameters shall be supported:

– For $(N,K) = (144,128)$ the following values for M and I shall be supported:
$I = 36$ and M between 2 and 52.

– For $(N,K) = (240,224)$ the following values for M and I shall be supported:
$I = 30$ and M between 2 and 62.

(VDSL1 Section 8.4)

XI. PRIOR ART ANALYSIS

521. It is my opinion that claims 9 and 13 of the ’882 Patent and claim 5 of the ’048 Patent are invalid based on (1) Mazzoni in view of VDSL1; (2) Mazzoni in view of LB-031; and (3) Fadavi-Ardekani in view of VDSL1. These claims have almost identical elements, so the element-by-element invalidity analysis is presented for all three claims together.

A. The combination of Mazzoni in view of VDSL1 renders obvious Claims 9 and 13 of the ’882 Patent and claim 5 of the ’048 Patent.

522. These claims have almost identical elements, so the element-by-element invalidity analysis is presented for all three claims together. It is not significant that claim 13 of the ’882 Patent and claim 5 of the ’048 Patent states that the message specifies a maximum number of bytes

of memory allocated to a *deinterleaver* rather than an *interleaver* as in claim 9 of the '882 Patent because the claims state "transmitting or receiving." For example, when the VTU-R transmits R-MSG2, which contains the "[m]aximal interleaver memory" to VTU-O, the VTU-O receives said message. Because VTU-R was transmitting a message indicating the maximal interleaver memory on the VTU-R, the VTU-O was necessarily receiving a message indicating the maximal deinterleaver memory on the VTU-O. Such a result is because the deinterleaver in the upstream must necessarily have the same memory as the interleaver in the upstream, and the deinterleaver in the downstream must necessarily have the same memory as the interleaver in the downstream. *See, e.g.*, VDSL1 at Table 8-1 (disclosing calculating the "(De)interleaver memory size" using equation MxIx(I– 1)/2); Mazzoni at 8:3-5 ("Of course, everything just described here for the terminal TO applies to the terminal TU with deinterleaving means with I branches and interleaving means with I′ branches.").

1. Preamble

523. The preamble of claims 9 and 13 of the '882 patent, and claim 5 of the '048 patent are presented in the table below:

Preamble of claim 9 and 13 of '882 Patent and claim 5 of '048 Patent
'882 claim 9 preamble: A system that allocates **shared memory** comprising: a **transceiver** that performs:
'882 claim 13 preamble: A system that allocates **shared memory** comprising: a **transceiver** that performs:
'048 claim 5 preamble: A system that allocates **shared memory** comprising: a **transceiver** that is capable of:

524. The court has construed the terms (shown in bold face in the table above) "shared memory" and "transceiver" (shown in bold face in the table above) as construed in the table below. I have used these terms as construed by the court in my analysis.